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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

AMITABH JAIN ET AL.

Serial No. 10/816,776 (TI-34913AA)

Filed April 2, 2004

For: ULTRA SHALLOW JUNCTION FORMATION

Art Unit 2813

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4-11-06

Jay M. Cantor, Reg. No. 19,906

Sir:

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences.

STATUS OF CLAIMS

This is an appeal of claims 1 to 18, all of the rejected claims. Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

A response was not filed after final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

The invention relates to a method for forming ultra shallow junctions in a semiconductor substrate. In order to form ultra shallow junctions, it is essential to retain implanted dopant close to the surface of the device with high active dopant concentrations after the annealing procedure. Prior art annealing procedures have resulted in greater dopant migration away from the device surface than provided by the present invention, thereby resulting in increased short channel effects as compared with the procedure of the present invention. In accordance with the method of the present invention, a dopant species is implanted into the semiconductor substrate with the implanted region optionally being made amorphous either prior to or subsequent to the implant. A low temperature anneal may take place to crystallize the amorphous region and then a second annealing of the implanted semiconductor substrate takes place with a ultra high temperature anneal comprising annealing temperatures from 1050°C to 1350°C for a period of from 0.5 to 3 milliseconds. Diffusion of the implanted dopant species is limited by the short times of the ultra high temperature (UHT) (1050°C to 1350°C) anneal and the resulting active dopant concentration is high due to the high temperatures of the UHT anneal (page 8, line 14ff).

GROUNDS OF REJECTION

Claims 1 to 3, 5, 7 to 9, 11 to 13 and 15 to 18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Mayur (U.S. 2003/0040130A1).

ARGUMENT

Claims 1 to 3, 5, 7 to 9, 11 to 13 and 15 to 18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Mayur (U.S. 2003/0040130A1). The rejection is without merit.

Claim 1 requires, among other features, the step of annealing the implanted semiconductor with a ultra high temperature anneal comprising annealing temperatures from 1050°C to 1350°C. for from about 0.5 to about 3 milliseconds. Mayur teaches an implant anneal at a temperature of greater than 1300K which as about 1026C for a duration of less than 50 milliseconds (paragraph 0007).

As noted in the Summary of Claimed Subject Matter, the intent of the subject invention is to create an ultra shallow junction in a semiconductor device. This is accomplished by an anneal process using a combination of very high temperature and very short duration. The claimed ultra high temperature range of the anneal is higher than any temperature suggested by Mayur and the duration of the anneal at the ultra high temperature is substantially less than suggested by Mayur (less than 50 milliseconds as opposed to 0.5 to 3 milliseconds). It is this combination which provides for the ultra shallow junction which cannot be obtained by any combination of temperature and anneal time suggested by Mayur. The differences over Mayur, especially in the anneal time, are so vast as to be beyond any reasonable suggestion that the differences are to be expected. Clearly, when the purpose of the invention is not contemplated by Mayur and the

conditions are vastly different from those suggested by Mayur, non-obviousness is readily apparent.

The above argument applies as well to independent claims 5, 9 and 13 as well as to the claims that depend therefrom.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,

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CLAIMS APPENDIX

The claims on appeal read as follows:

1. A method for forming ultra shallow junctions, comprising:

providing a semiconductor;

implanting a dopant species into said semiconductor; and

annealing said implanted semiconductor with a ultra high temperature anneal comprising annealing temperatures from 1050°C to 1350°C. for from about 0.5 to about 3 milliseconds.

2. The method of claim 1 further comprising an amorphizing implant.

3. The method of claim 2 wherein said amorphizing implant comprises implanting a species from the group consisting of silicon, germanium, antimony, indium, arsenic, neon, argon, krypton, and xenon.

5. A method for forming junction in integrated circuits, comprising:

providing a semiconductor;

forming a patterned photoresist layer on said semiconductor;

implanting dopant species into said semiconductor;

removing said patterned photoresist layer;

annealing said implanted semiconductor with a solid phase epitaxy anneal; and

annealing said implanted semiconductor with a ultra high temperature anneal comprising annealing temperatures from 1100°C to 1350°C. for from about 0.5 to about 3 milliseconds.

7. The method of claim 6 further comprising an amorphizing implant.

8. The method of claim 7 wherein said amorphizing implant comprises implanting a species from the group consisting of silicon, germanium, antimony, indium, arsenic, neon, argon, krypton, and xenon.

9. A method of forming a MOS transistor, comprising:

providing a semiconductor substrate;

forming a gate dielectric layer on said semiconductor;

forming a gate electrode on said gate dielectric layer;

implanting dopant species into said semiconductor adjacent to said gate electrode;

annealing said implanted semiconductor with a solid phase epitaxy anneal at a temperature between 550°C and 950°C; and

annealing said implanted semiconductor with a ultra high temperature anneal comprising annealing temperatures from 1100°C to 1350°C. for from about 0.5 to about 3 milliseconds.

11. The method of claim 10 further comprising an amorphizing implant performed prior to said implanting of said dopant species.

12. The method of claim 11 wherein said amorphizing implant comprises implanting a species from the group consisting of silicon, germanium, antimony, indium, arsenic, neon, argon, krypton, and xenon.

13. A method of forming an integrated circuit MOS transistor, comprising:

providing a semiconductor substrate;

forming a gate dielectric layer on said semiconductor;

forming a gate electrode on said gate dielectric layer;

implanting first dopant species into said semiconductor adjacent to said gate electrode;

forming sidewall structures adjacent to said gate electrode;

implanting second dopant species into said semiconductor adjacent to said sidewall structures; and

annealing said implanted semiconductor with a ultra high temperature anneal comprising annealing temperatures from 1100°C to 1350°C. for from about 0.5 to about 3 milliseconds.

15. The method of claim 14 further comprising an amorphizing implant performed prior to said implanting of said first dopant species.

16. The method of claim 15 further comprising an amorphizing implant performed prior to said implanting of said second dopant species.

17. The method of claim 13 further comprising an amorphous implant performed prior to said implanting of said second dopant species.

18. The method of claim 16 wherein said amorphizing implants comprises implanting a species from the group consisting of silicon, germanium, antimony, indium, arsenic, neon, argon, krypton, and xenon.

EVIDENCE APPENDIX

Not applicable

RELATED PROCEEDINGS APPENDIX

Not applicable